PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
THOMAS J. SONDERMAN
PIRAINDER LALL

Serial No.: 10/614,354

Filed: July 7, 2003

For: METHODS OF CONTROLLING PROPERTIES AND CHARACTERISTICS OF A GATE INSULATION LAYER BASED UPON ELECTRICAL TEST DATA, AND SYSTEM FOR PERFORMING SAME

Confirmation No.: 7900

Group Art Unit: 2823

Examiner: Khiem D. Nguyen

Atty. Dkt. No.: 2000.100800/TT5273

Customer No.: 23720

CORRECTED APPEAL BRIEF

MS APPEAL BRIEF - PATENTS
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this Corrected Appeal Brief to the Board of Patent Appeals and Interferences in response to the Notification of Non-Compliant Appeal Brief dated August 1, 2006. The Final Office Action was dated March 31, 2006, and the Notice of Appeal was filed on May 17, 2006.

No fees are believed to be due in connection with this Corrected Appeal Brief. However, should any fees be required, the Director is authorized to deduct such fees from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.100800.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-22 were originally filed with this application. Claims 1, 3, 6-9, 11-15, 21 and 22 are currently pending in the application. Claims 2, 4-5, 10 and 16-20 were canceled in Applicants' response to the January 13, 2005 Office Action. Claims 1, 3, 6-9, 11-15, 21 and 22 were rejected in the Final Office Action issued on March 31, 2006. Claims 1, 3, 6-9, 11-15, 21 and 22 are the subject of the present appeal. Claims 1, 3, 6-9, 11-15, 21 and 22 are attached as Appendix A.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention is directed to semiconductor fabrication technology, and, more particularly, to various methods of controlling properties and characteristics of a gate insulation layer based upon electrical test data, and a system for performing same. There are four independent claims at issue in the current appeal: claims 1, 9, 21 and 22.

Independent claim 1 is generally directed to a method that involves performing at least one electrical test on at least one flash memory device 10 to determine a duration of a programming cycle performed on the flash memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed flash memory device 10 based upon the determined duration

of the programming cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed flash memory device 10. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

Independent claim 9 is generally directed to a method that involves performing at least one electrical test on at least one flash memory device 10 to determine a duration of an erase cycle performed on the flash memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed flash memory device 10 based upon the determined duration of the erase cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed flash memory device 10. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

Independent claim 21 is generally directed to a method that involves performing at least one electrical test on at least one memory device 10 to determine a duration of a programming cycle performed on the memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed memory device 10 based upon the determined duration of the programming cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed memory device 10. This invention is generally described throughout the specification. By way of example only, at

least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

Independent claim 22 is generally directed to a method that involves performing at least one electrical test on at least one memory device 10 to determine a duration of an erase cycle performed on the memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed memory device 10 based upon the determined duration of the erase cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed memory device 10. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3 6-9, 11-15, 21 and 22 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Fang (U.S. Patent No. 6,133,746).

VII. ARGUMENT

A. Legal Standards

As the Board well knows, an anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). To the extent the Examiner relies on principles of inherency in making the anticipation rejections in the Office Action, inherency requires that the asserted proposition necessarily flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981); *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1463-64 (Bd. Pat. App.

& Int. 1990); *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Int. 1987); *In re King*, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; see also *Skinner*, at 1789. "Inherency … may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Skinner*, at 1789, citing *Oelrich*. Where anticipation is found through inherency, the Office's burden of establishing prima facie anticipation includes the burden of providing "…some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Skinner* at 1789.

B. The Examiner Erred in Rejecting Claims 1, 3, 6-8 and 21

These claims are directed to methods of forming flash memory devices whereby the performance of the resulting devices may be enhanced. For example, independent claim 1 recites performing an electrical test to determine a duration of a programming cycle for the flash memory device. Claim 1 also recites that the act of determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed flash memory device is **based upon** the determined duration of the programming cycle. Claim 1 further recites the act of performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer on the subsequently formed flash memory device. Independent claim 21 is similar to claim 1 except

that claim 21 is directed to a generic "memory device" as opposed to the specifically identified "flash memory device" in claim 1.

It is respectfully submitted that the Examiner erred in asserting that Fang discloses the inventions set forth in these claims. Fang is directed to a method of testing gate oxide layers. More specifically, Fang is directed to a method of determining reliable gate oxide thicknesses by subjecting test transistors to an alternating current (AC) voltage until the transistors break down. Abstract. Fang specifically notes that the "conventional approach for determining the reliability of a transistor is to stress gate oxides of varying thickness under direct current (DC) conditions and project the gate oxide reliability for an industry standard ten-year lifetime." Col. 1, ll. 58-62 (emphasis added). Fang states that more realistic results can be obtained by stressing the gate oxide layer based upon AC stress conditions (as opposed to DC current conditions) because AC stress conditions are more consistent with the actual operating conditions of the transistor. Col. 3, ll. 9-17.

Fang discloses that the test structures are subjected to an AC stress voltage and the time or duration until breakdown occurs is measured. Col. 4, ll. 23-27. Thereafter, certain reliability parameters are determined from the reliability data, such as the measured breakdown times. Col. 4, ll. 36-48. Once the reliability parameters have been determined, the gate oxide for a ten-year lifetime is calculated. Col. 4, ll. 63-65.

In the Final Office Action, the Examiner asserted that Fang disclosed "determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said programming cycle" (citing Col. 1, lines 21-34). Final Office Action, p. 5. The Examiner goes on to restate Fang's description of how a flash memory cell is PROGRAMMED,

and concludes by asserting that the threshold voltage of the cell is the ELECTRICAL TEST recited in the pending claims. The Examiner continues by asserting that step 104 in Figure 1 of Fang ("Measure Breakdown Times under AC Stress Test") is the act of determining the duration of a programming cycle of the flash memory device recited in claim 1. Final Office Action, p. 2.

Applicants respectfully disagree with this reading and interpretation of Fang for many reasons. It is believed that the Examiner's fundamental misunderstanding or misreading of Fang and the subject matter of the pending claims is the basis for the errors identified herein.

In Col. 1, lines 21-34 (cited by the Examiner), Fang merely describes an illustrative example of how selected flash memory cells are PROGRAMMED. In general, memory devices operate by detecting the presence or absence of a stored electrical charge on the memory device. The threshold voltage of a transistor associated with the memory cell is DIFFERENT depending upon whether or not a charge is stored on the cell. These different threshold voltages (which differ depending upon whether a charge is stored in the cell or not) are used to READ information from the cell. In this manner, each individual cell can represent a "1" or a "0" (high or low) depending upon the threshold voltage of the transistor of the memory cell.

The Examiner clearly erred in asserting that the threshold voltage described in the identified passage of Fang is an ELECTRICAL TEST. This passage of Fang merely describes certain operational characteristics of a flash memory device. The only testing mentioned in Fang is of the gate insulation layers. Respectfully, the Examiner's rejection is based upon a fundamentally flawed analysis and an incorrect assumption.

The flawed analysis is further reflected in the Examiner's assertion that Fang's disclosure to "measure breakdown times under AC stress test" is the claimed act of measuring the duration of a programming cycle of a flash memory device. Fang describes an illustrative duration of a

programming cycle, *e.g.*, 200 μs, in the passage discussed immediately above. However, stressing the gate insulation of a memory device until it ruptures does not have anything to do with PROGRAMMING a flash memory cell.

As stated above, Fang is directed to stressing gate insulating layers using AC test conditions as opposed to DC test conditions. Fang does not remotely disclose or suggest the inventions set forth in claims 1, 3-8 and 21.

C. The Examiner Erred in Rejecting Claims 9, 11-15 and 22

Independent claim 9 is similar to independent claim 1 except that the electrical test is performed to determine the duration of an erase cycle for the flash memory device. Independent claim 22 is similar to claim 9 except that it is directed to a generic memory device as opposed to the flash memory device recited in claim 9.

The errors identified above with respect to claims 1 and 21 apply equally with respect to the Examiner's rejection of these claims. In addition, the Examiner failed to specifically identify where Fang discloses anything relating to an erase cycle of a memory device. The reason that there is no such identification is because Fang simply does not mention erase cycle times for a memory device. Accordingly, as a matter of law, the Examiner's anticipation rejection of these claims is legally improper.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1, 3, 6-9, 11-15, 21 and 22 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

Applicants do not rely upon any evidence as indicated on the attached Evidence Appendix.

X. RELATED PROCEEDINGS APPENDIX

There are no Related Proceedings for this appeal as indicated on the attached Related Proceedings Appendix.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing claims 1, 3, 6-9, 11-15, 21 and 22 over the prior art of record. Applicants respectfully request the Board reverse the Examiner's rejections. The undersigned attorney may be contacted at (713) 934-4055 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

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Date: August 14, 2006

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APPENDIX A

1. A method, comprising:

performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle performed on said flash memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed flash memory device.

3. The method of claim 1, wherein performing said at least one electrical test on said at least one flash memory device further comprises performing said at least one electrical test on said at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and an erase cycle time.

6. The method of claim 1, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

7. The method of claim 1, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

8. The method of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

9. A method, comprising:

performing at least one electrical test on at least one flash memory device to determine a duration of an erase cycle performed on said flash memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed flash memory device.

11. The method of claim 9, wherein performing said at least one electrical test on said at least one flash memory device further comprises performing said at least one electrical test on said at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and a programming cycle time.

12. The method of claim 9, wherein said memory device is comprised of a gate insulation layer, a floating gate layer positioned above said gate insulation layer, an intermediate

insulation layer positioned above said floating gate layer, and a control gate layer positioned above said intermediate insulation layer.

13. The method of claim 9, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

14. The method of claim 9, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

15. The method of claim 9, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

21. A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of a programming cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.

22. A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of an erase cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.

EVIDENCE APPENDIX

Applicants do not rely on any evidence for this appeal.

RELATED PROCEEDINGS APPENDIX

There are no Related Proceedings for this appeal